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IN THE CLAIMS:

Please cancel claims 11-18 and amend the remaining claims as follows:

1. (Currently Amended) An apparatus for maintaining signal integrity between integrated circuits residing on a printed circuit board, said apparatus comprising:

adjustable delay circuitry within said circuits, said adjustable delay circuitry ~~being adapted to adjust~~ adjusting timing of signals processed within said circuits;

[[;]]

a phase monitor connected to said circuits, said phase monitor ~~being adapted to detect~~ detecting phase differences between signals output by said circuits; and

~~a controller~~ delay time set registers connected to said delay circuitry and said phase monitor, said ~~controller being adapted to adjust~~ delay time set registers adjusting ~~said delay~~ circuitry to compensate for said phase differences.

2. (Currently Amended) The apparatus in claim 1, further comprising:

first data lines connecting said circuits to each other; and

second data lines connecting said ~~controller~~ delay time set registers to said circuits,

wherein said second data lines transmit data at a slower rate than said first data lines.

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3. (Currently Amended) The apparatus in claim 1, further comprising a serial data line connecting said ~~controller~~ delay time set registers to said circuits.

4. (Currently Amended) ~~The apparatus in claim 1,~~ An apparatus for maintaining signal integrity between integrated circuits residing on a printed circuit board, said apparatus comprising:

adjustable delay circuitry within said circuits, said adjustable delay circuitry adjusting timing of signals processed within said circuits;

a phase monitor connected to said circuits, said phase monitor detecting phase differences between signals output by said circuits; and

a controller connected to said delay circuitry and said phase monitor, said controller adjusting said delay circuitry to compensate for said phase differences,

wherein at least one of said circuits comprises a receiver circuit, said receiver circuit comprising:

a plurality of channels; and

a configuration word interface connected to said channels and to said controller,

wherein said adjustable delay circuitry comprises at least one adjustable delay device within each of said channels, and

wherein said configuration word interface controls said delay device to coordinate a signal timing of said channels.

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5. (Currently Amended) The apparatus in claim 4, further comprising delay registers between said delay device and said configuration word interface, wherein said delay registers ~~are adapted to~~ store information regarding timing delay of an associated delay device.

6. (Currently Amended)The apparatus in claim 4, wherein said configuration word interface is connected to said controller and said controller ~~is adapted to supply~~ supplies information to control said delay device.

7. (Original) The apparatus in claim 4, wherein said configuration word interface permits dynamic control of said delay device.

8. (Original) The apparatus in claim 4, wherein said configuration word interface includes a phase voltage converter.

9. (Original) The apparatus in claim 4, wherein said adjustable delay device comprises:

a resistor-capacitor network;

a Schmitt trigger connected to said resistor-capacitor network; and

a digital-to-analog converter connected to said resistor-capacitor network.

10. (Original) The apparatus in claim 4, wherein said adjustable delay device comprises:

a resistor-capacitor network;

variable transistors connected to said resistor-capacitor network; and

a digital-to-analog converter connected to said resistor-capacitor network.

11-18. (Canceled).

19. (Currently Amended) A method of coordinating timing signals within circuits on a printed circuit board, said method comprising:

detecting phase differences between signals output by said circuits using a phase monitor; and

adjusting delay circuitry within said circuits to compensate for said phase differences using ~~a controller~~ delay time set registers.

20. (Currently Amended) The method in claim 19, wherein first data lines connecting said ~~controller~~ delay time set registers to said circuits transmit data at a slower rate than second data lines connecting said circuits to each other.

21. (Currently Amended) The method in claim 19, further comprising using a serial data line to connect said ~~controller~~ delay time set registers to said circuits.

22. (Currently Amended) ~~The method in claim 19,~~ A method of coordinating timing signals within circuits on a printed circuit board, said method comprising:

detecting phase differences between signals output by said circuits using a phase monitor; and

adjusting delay circuitry within said circuits to compensate for said phase differences

using a controller,

wherein at least one of said circuits comprises a receiver circuit, and said adjusting process comprises transmitting control information from said controller through a configuration word interface to said delay devices to coordinate a signal timing of said channels.

23. (Original) The method in claim 22, further comprising dynamically controlling said delay circuitry using said configuration word interface.

24. (Original) The method in claim 19, further comprising storing delay information in delay registers.